# Final Report:

Project Final Report.pdf

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Subthreshold Data Path Circuit Design:
Two Implementations of Low Power Simple Adder

**Project Overview:**

For this project I will be doing two different implementations of a simple 8 bit program controller. The circuits will have the same topology, but one adder will be built using static CMOS construction, the other using dynamic CMOS construction. The circuit will be an 8 bit adder with one input connected to a static input of 00000001, the other input will be connected to a 2-to-1 flip-flopped Mux. The Mux will control whether the input to the adder will be the previous sum or a jump to value. This is designed to simulate the program control that would be required to continuously read from a memory address such as in a portable music player, but have the ability to skip(jump) to the next song in memory. The design however failed to perform as expected.

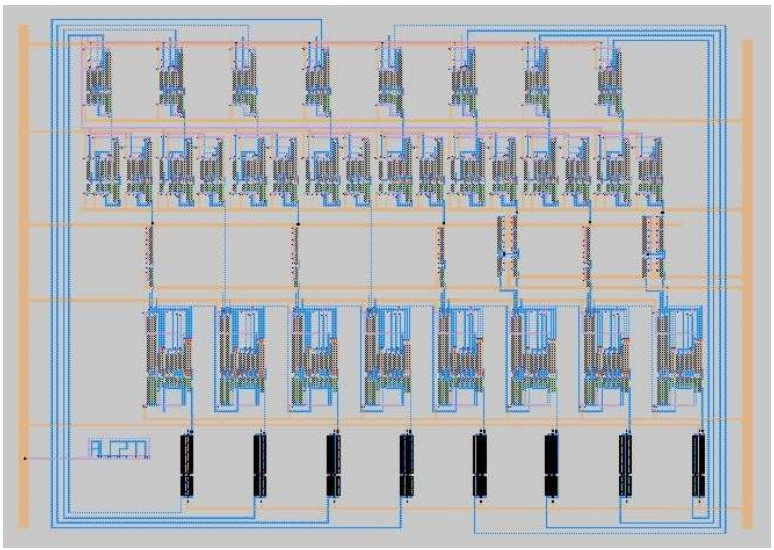


Figure 22. Static CMOS Layout

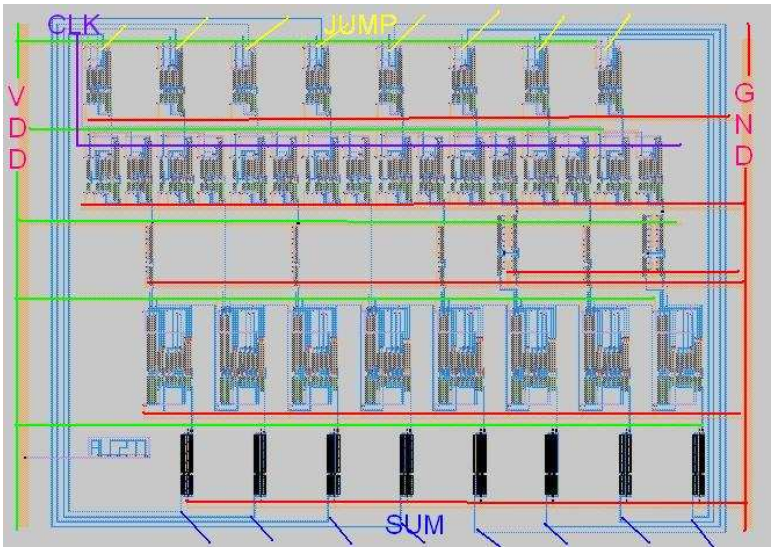
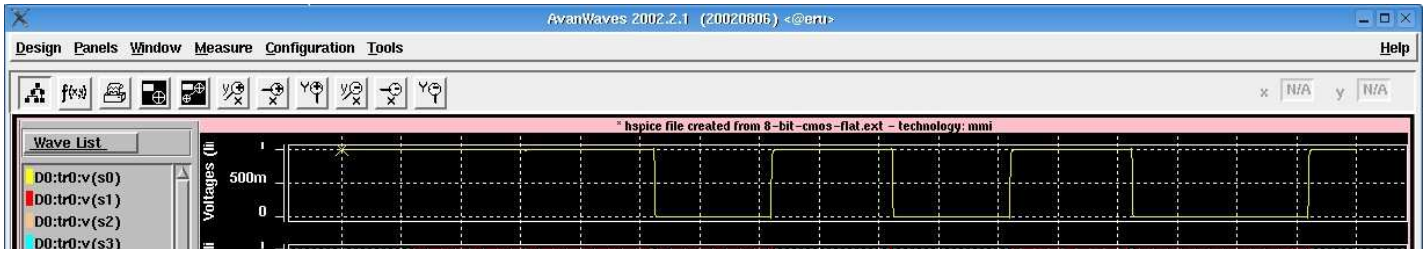



Figure 23. Static CMOS Layout With I/Os Labeled

The design was 159.100 X 111.730, but was plauged with problems. The counter never quite functioned correctly with the flip flops in place. The system had inputs for VDD, GND, clock, JUMP input, and a 8 bit input for Jump Address. The counter does count to about 4 and then loses it self once the carryout is passed.



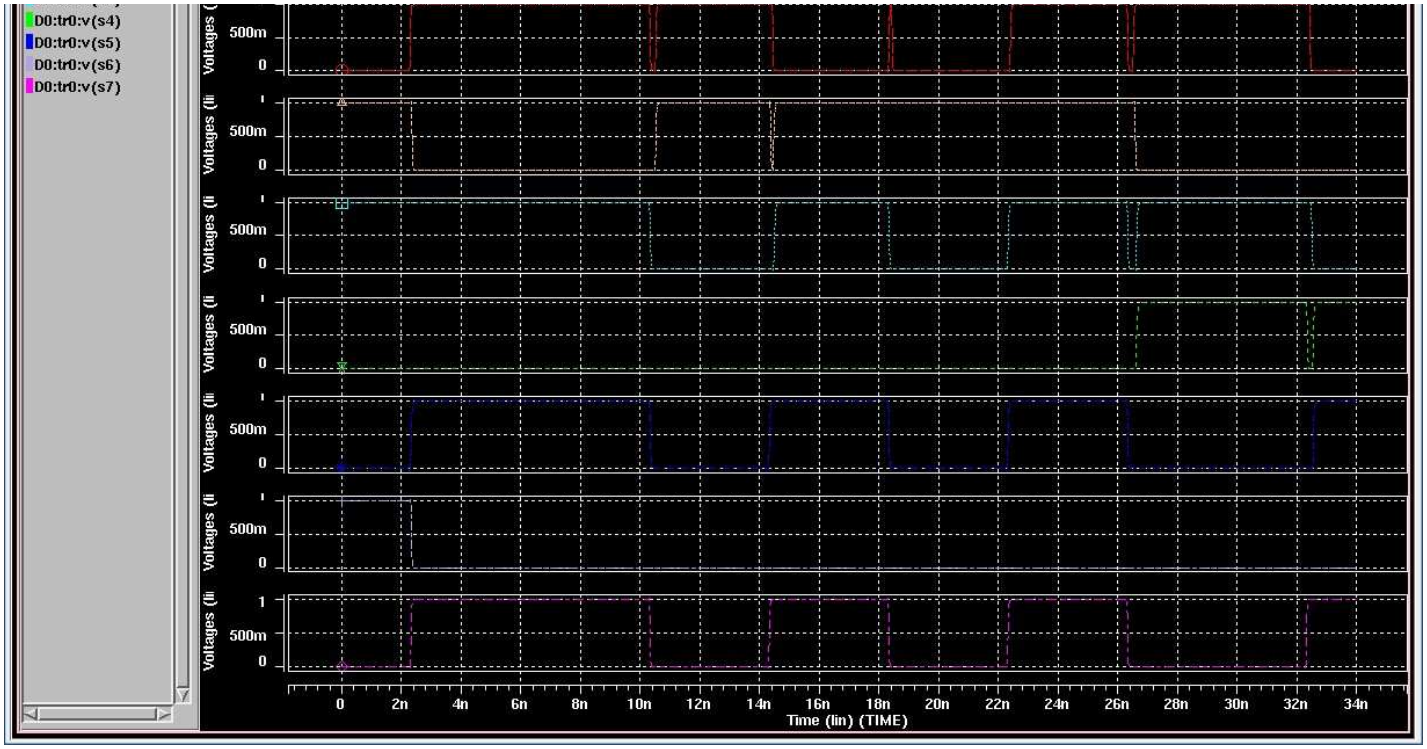



Figure 24. Static CMOS Awaves Output

The layouts were optimized by making sure each component fit nearly the same form factor when placed on the grid. This allowed the GND and VDD lines to be easily placed going horizontally in an evenly spaced out manner. By using a cascading adder design, in which the carry's are not put through an inverter between each adder, I was able to reduce the area needed. The transistors were sized to the proper size for the mirror adders to insure optimum performance and to balance the upswing and downswing charactaristics.

**Conclusions**

To make a comparision between the dynamic and static CMOS designs as the correspond to power usage, I will examine the single bitter adders when they are not connected to the rest of the system. The static CMOS design uses less dynamic power, and because the counter is switching constantly very little static power will be dissipated. As you can see in the graph below, there are biggest reductions in the power consuption when we use sub threshold design. You can see the change in the curve as the VDD approaches Vt.

| Supply (V) | Static CMOS Avg (W) | Static CMOS Max (W) | Static CMOS RMS (W) | Dynamic CMOS Avg (W) | Dynamic CMOS Max (W) | State CMOS RMS (W) |
|---|---|---|---|---|---|---|
| 1.0 | 2.62E-06 | 1.23E-03 | 3.25E-05 | 5.94E-06 | 1.50E-03 | 6.48E-05 |
| 0.8 | 1.33E-06 | 5.64E-04 | 1.56E-05 | 2.70E-06 | 6.10E-04 | 2.81E-05 |
| 0.6 | 6.89E-07 | 2.57E-04 | 7.33E-06 | 1.34E-06 | 2.97E-04 | 1.24E-05 |
| 0.4 | 3.25E-07 | 9.84E-05 | 2.66E-06 | 6.24E-07 | 1.05E-04 | 4.30E-06 |
| 0.3 | 1.85E-07 | 2.50E-05 | 9.82E-07 | 3.69E-07 | 4.27E-05 | 1.80E-06 |
| 0.2 | 8.21E-08 | 3.22E-06 | 2.05E-07 | 1.59E-07 | 3.94E-06 | 3.72E-07 |
| 0.1 | 1.19E-08 | 2.06E-07 | 1.78E-08 | 1.78E-08 | 1.98E-07 | 2.29E-08 |

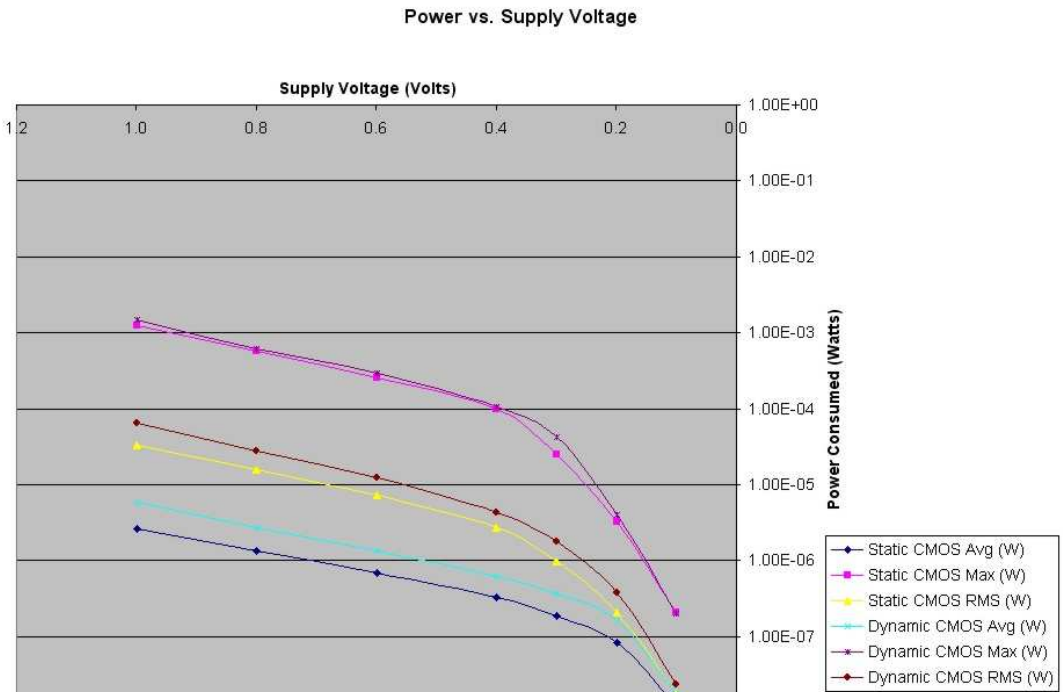



Figure 25. Power Comparison

Here are the two circuits operating at below threshold:

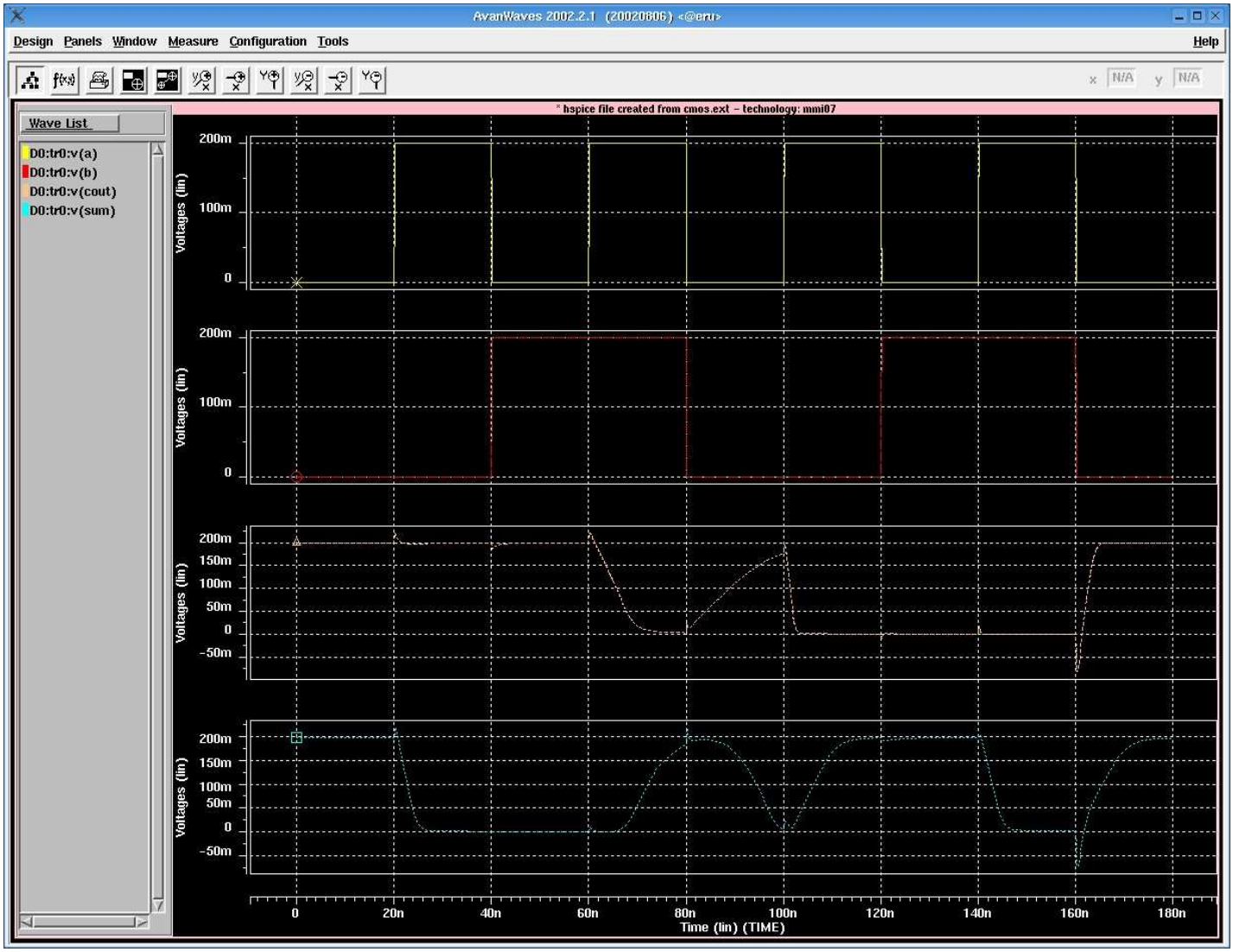
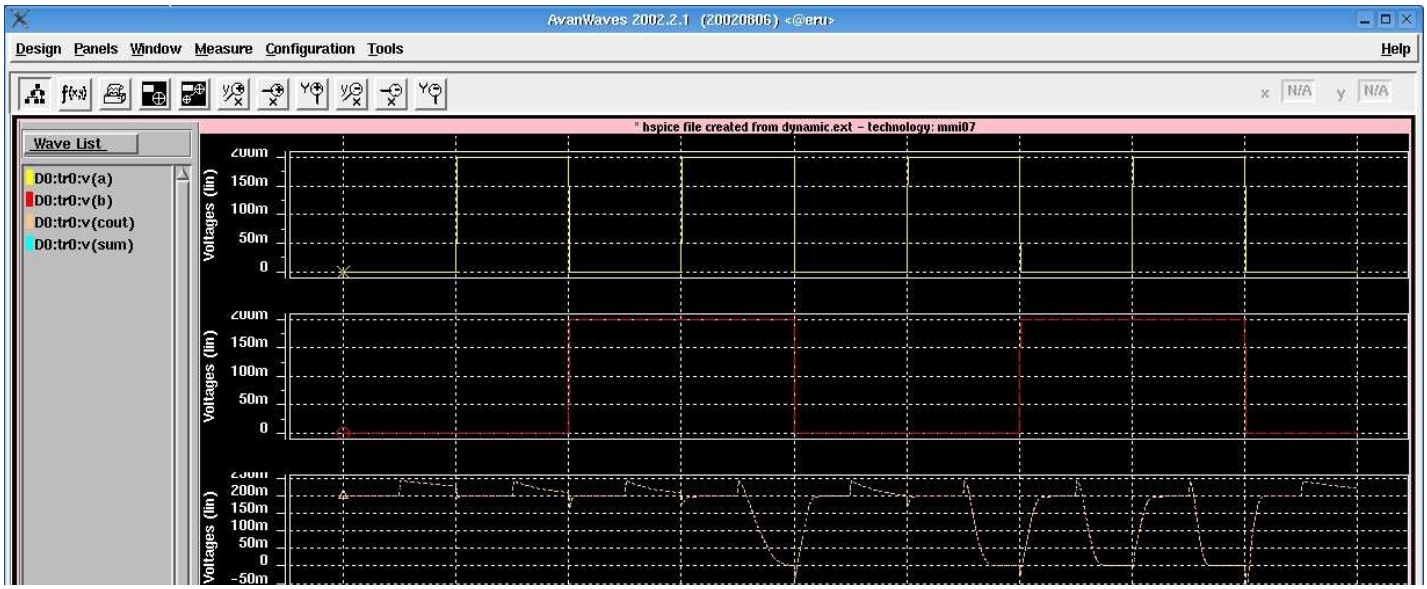



Figure 26. Static CMOS at .02V VDD



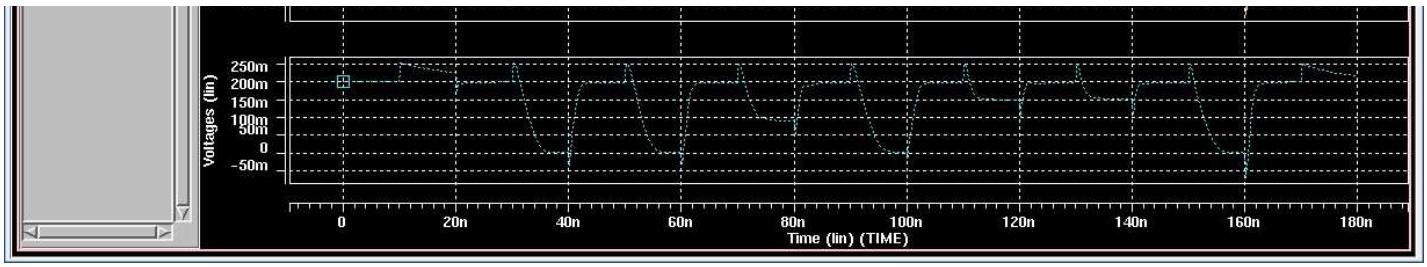



Figure 25. Dynamic CMOS at .02V VDD