Proposal:

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Project Description:

Power consumption is becoming an ever increasing problem in today's laptops, cellular telephones, and portable music players.

This project will look at the effects of operating two simple 8 bit ripple carry adder designs at a very low sub threshold supply voltage. One design will be a static CMOS design, and one will be a dynamic CMOS design. The goal of this project is to deduce which method of construction will give the best performance while consuming the least amount of power. It is possible that the circuit may also consume the least power vs. speed of operation at a point not at the minimum supply voltage.

This adder could be used to control the access to music from either an optical disc or internal memory. This application will be used as the basis for the minimum operating characteristics. For a simple mp3 player the adder would need to address memory much like a program counter with a constant being added with the ability to jump. Most mp3 are encoded at 128kbps and 44.1 kHz. In the same way a CD player samples the data on the disc at 44.1 kHz, so if the simple adder where to be used in an audio device to control what would play (not decoding the signal) it must operate at least that speed, if not higher.
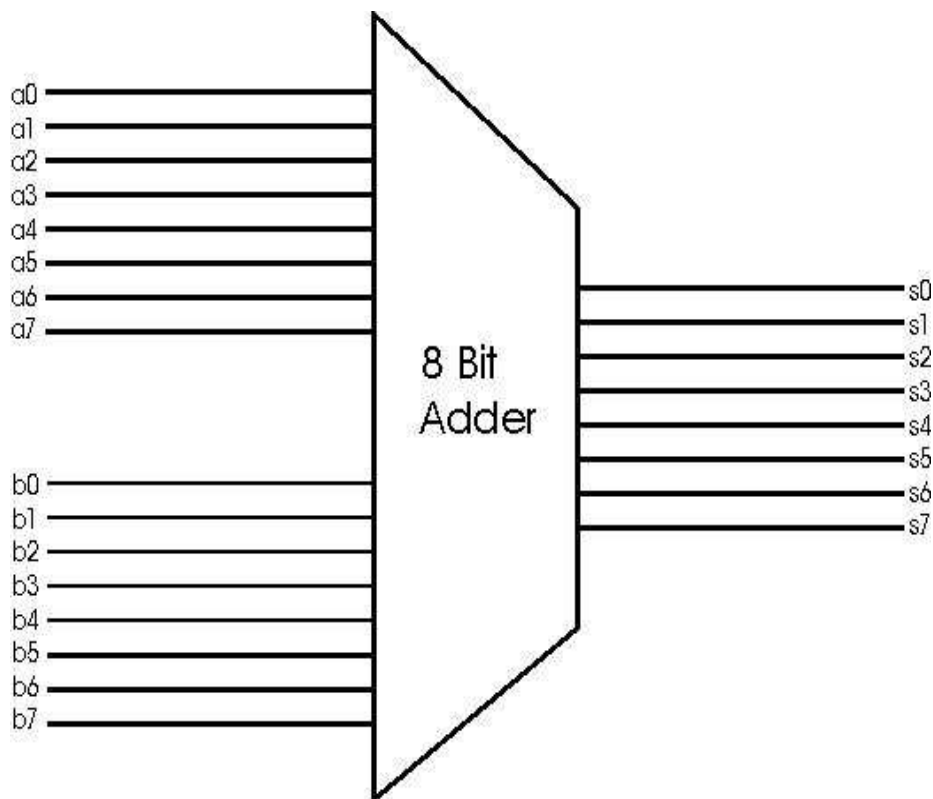
Project Floor Plan:

Figure 1. 8 Bit Adder

The two designs will both have the same topology, they will be 8 full single bit adders chained together. The total circuit will have 2-8 bit words as inputs, a carry in, a carry out. That makes for a total of 18 inputs. The circuit will output the sum and a carry out, for a total of 9 outputs.

The adder will be connected to a constant input and with a 2-to-1 Mux to give the ability for the circuit to select the previous sum, or jump to another input.
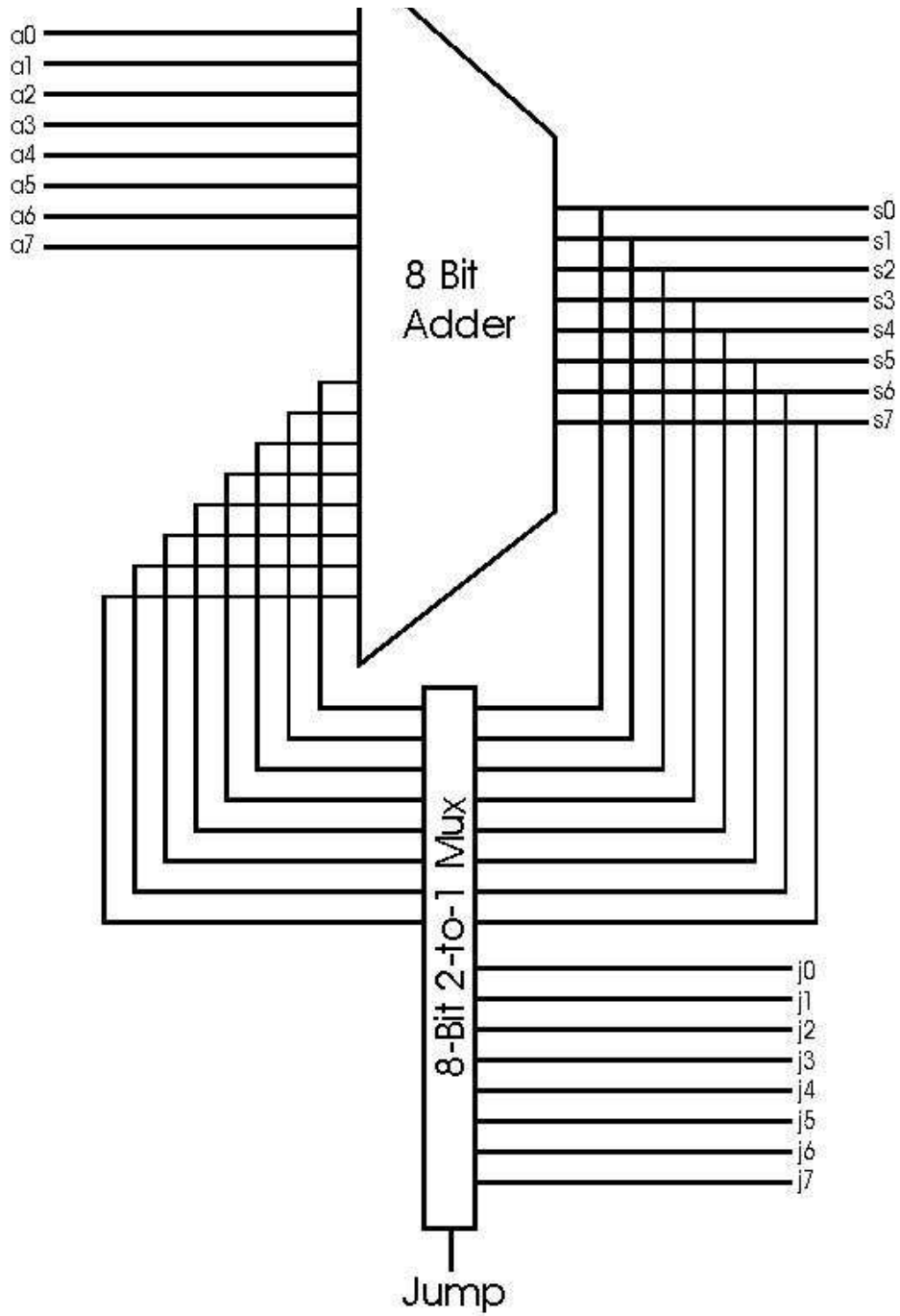
Figure 2. 8 Bit Adder With 2-to-1 Mux Allowing For Jump

The other project member is no longer enrolled in the class, so Andrew Cassell will be responsible for all design and testing.