Project Prototype:

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Subthreshold Data Path Circuit Design:
Two Implementations of Low Power Simple Adder

Project Overview:

For this project I will be doing two different implementations of a simple 8 bit program controller. The circuits will have the same topology, but one adder will be built using static CMOS construction, the other using dynamic CMOS construction. The circuit will be an 8 bit adder with one input connected to a static input of 00000001, the other input will be connected to a 2-to-1 flip-flopped Mux. The Mux will control whether the input to the adder will be the previous sum or a jump to value. This is designed to simulate the program control that would be required to continuously read from a memory address such as in a portable music player, but have the ability to skip(jump) to the next song in memory.

1 Bit 2-to-1 Mux:

For the prototype I used a two stage NAND implementation of the Multiplexor.

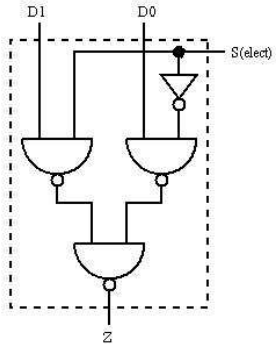


Figure 10. 1 Bit 2-to-1 Multiplexor (Choi)

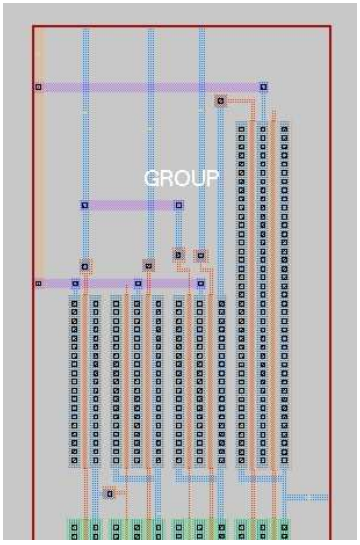
Inputs and Outputs

Type	Name	Description
Input	D0	Data Input Selected When Sel goes Low
Input	D1	Data Input Selected When Sel goes High
Input	Sel	Selects Which Data is Connected to Output
Output	Z	Data Output

Specifications

Measure	Value
Width	6.8
Length	17.37
Avg Power	3.92µW
Peak Power	1.38mW
Supply Voltage	1V

The Power supply rails extend on the left beyond the upper and lower bounds of the transistor layout to accommodate power rails. Inputs are taken from a metal layer.



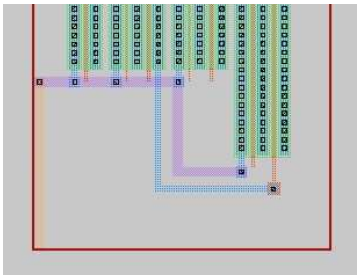


Figure 12. 2-to-1 Multiplexor VLSI Max Design

The block will receive a VDD of 1V during the final design to isolate the effects of the subthreshold testing to the add data path. Speed as a result should be no problem.

The following graph shows the 2-to-1 Multiplexor operating correctly, for all of the possible inputs. Not all of the possible transitions were considered, because this portion of the circuit should be much faster than the rest of the circuit as it will be operating above the threshold. The Z output follows the d0 input while the sel line is at 0, and then follows d1 when sel is at 1.

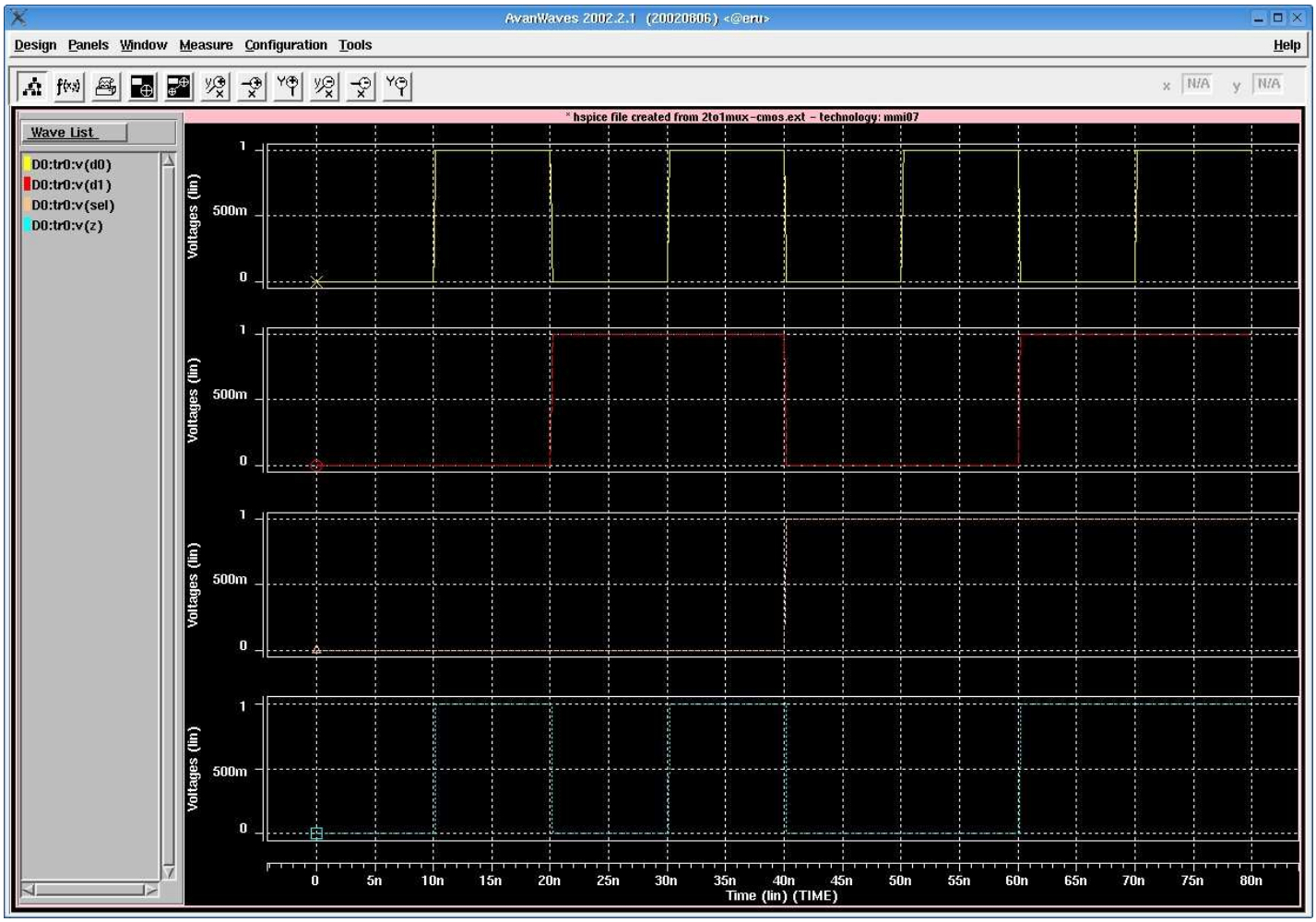


Figure 13. Awaves Output Plot of the 2-to-1 Mux

Files Related to the 2-to-1 Multiplexor:

Description	Link
Max Layout	2to1mux-cmos.max
HSpice	2to1mux-cmos.sp
Inputs	2to1mux-cmos.hsp
Measures	2to1mux-cmos.mto

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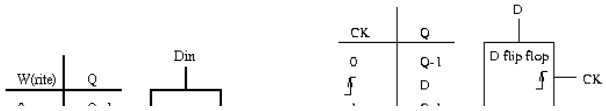
1 Bit D-Flip-Flop

Using the design of the 2-to-1 Mux a D-latch was first constructed, and then used to create a positive edge triggered flip-flop.



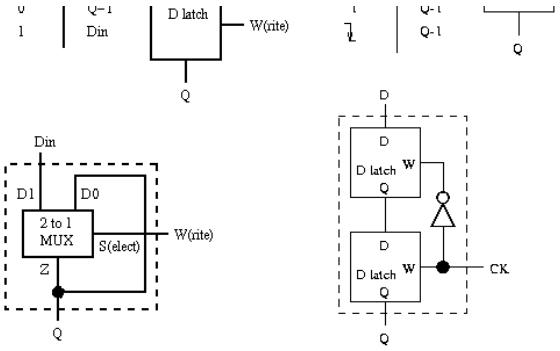


Figure 14. D Flip Flop(Choi)

Inputs and Outputs

Type	Name	Description
Input	D	Data Input
Input	Clock	Triggers the Data to be read on rising edge
Output	Q	Data Output

Specifications

Measure	Value
Width	14.85
Length	17.40
Avg Power	6.10µW
Peak Power	2.57mW
Supply Voltage	1V

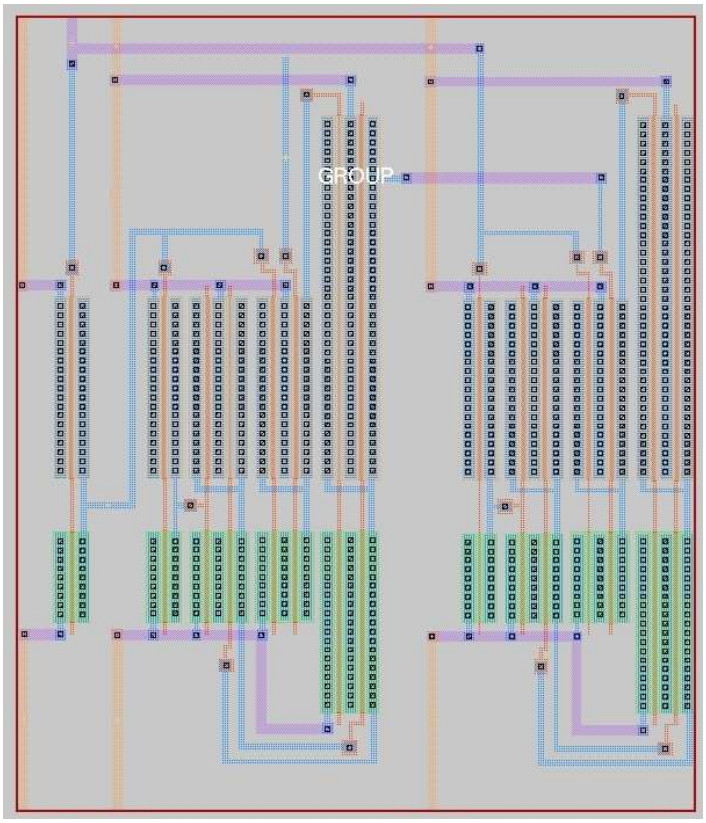


Figure 15. D Flip Flop VLSI Design

The block will receive a VDD of 1V during the final design to isolate the effects of the subthreshold testing to the add data path. Speed as a result should be no problem.

The following graph shows the D flip flop operating correctly, for all of the possible inputs. Not all of the possible transitions were considered, because this portion of the circuit should be much faster than the rest of the circuit as it will be operating above the threshold. The Q output follows the d input when the there is a rising clock edge.

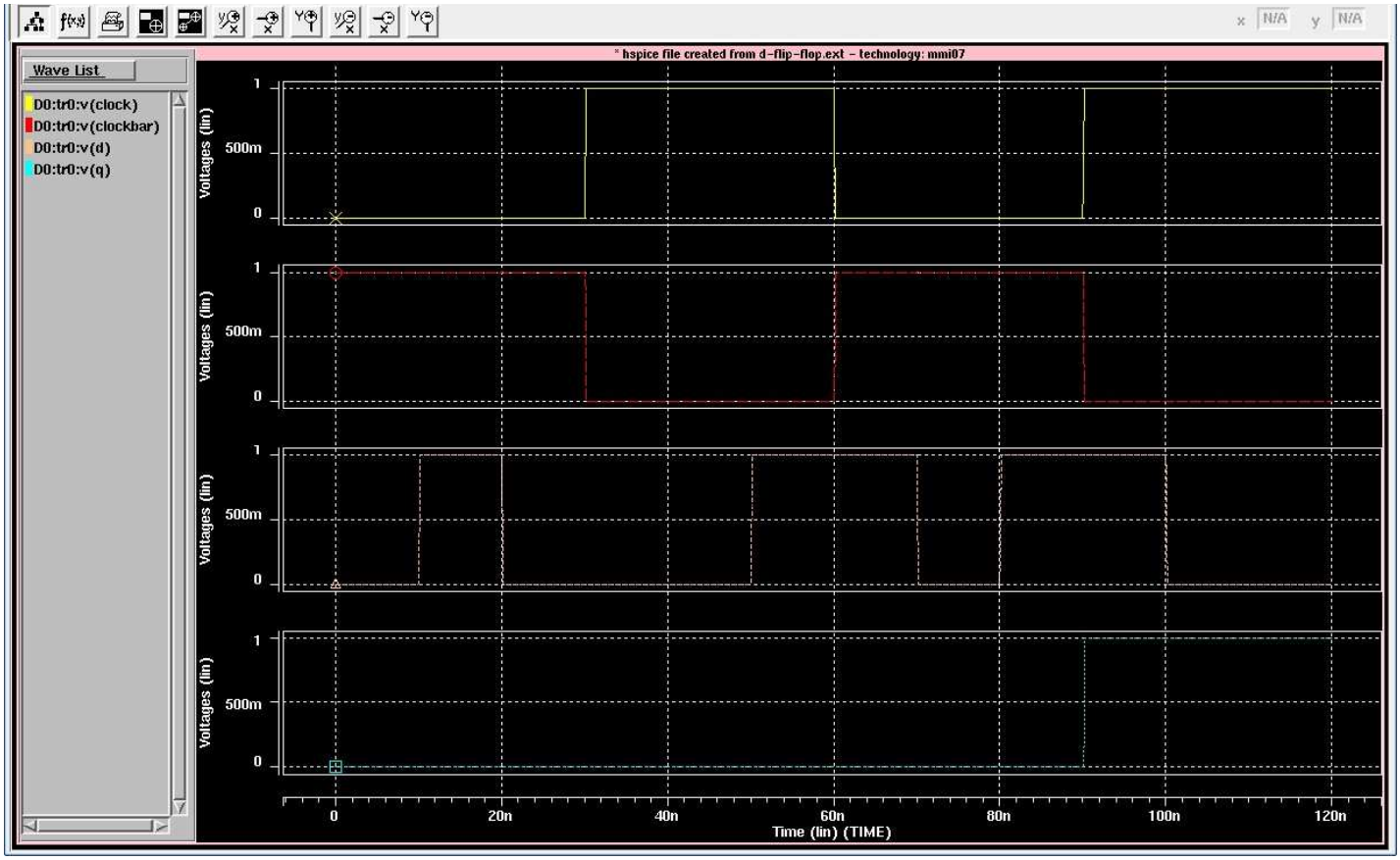


Figure 16. Awaves Output of the D Flip Flop Test

Files Related to the D Flip Flop:

Description	Link
Max Layout	D-flip-flop.max
HSpice	D-flip-flop.sp
Inputs	D-flip-flop.hsp
Measures	D-flip-flop.mto

Static CMOS 1 Bit Mirror Adder:

The prototype is a 1 bit full mirror adder designed in static CMOS.

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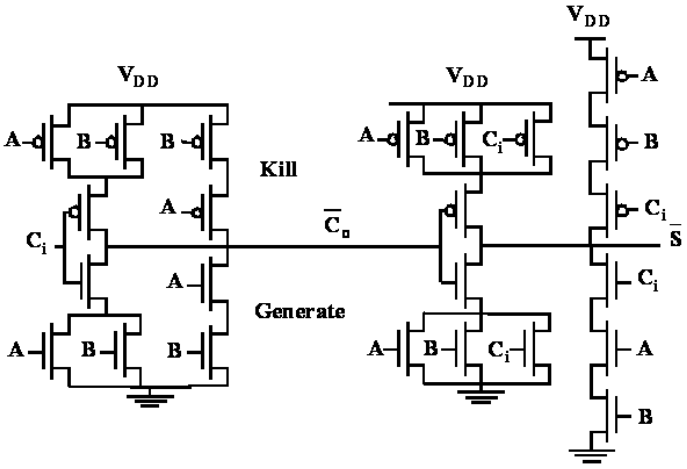

Figure 17. The Mirror Adder

Inputs and Outputs

Type	Name	Description
Input	A	Data Input
Input	B	Data Input
Input	Cin	Carry In
Output	Cout	Carry Out
Output	Sum	Sum

Specifications

Measure	Value
Width	10.69
Length	21.16
Avg Power	4.47μW
Peak Power	0.89mW
Supply Voltage	1V

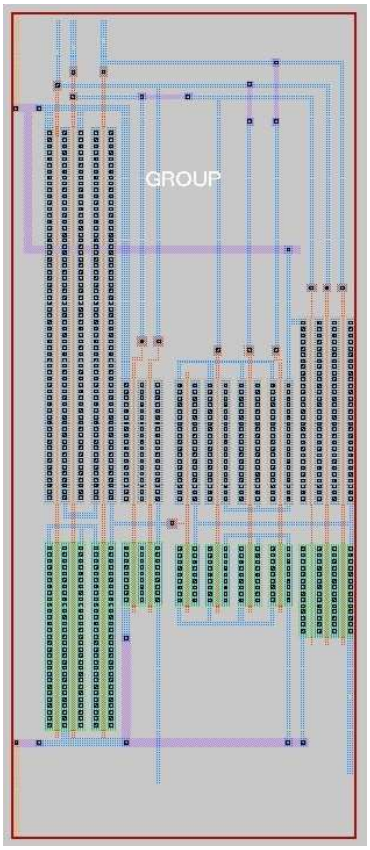

Figure 18. The Mirror Adder VLSI Design

The following graph shows the cmos adder operating correctly, for all of the possible inputs at a supply voltage of 1V. Speed was not considered because the design is going to focus on achieving to lowest power which the greatest speed for an operating block of 8 units.

Note: Cin and Sum in the plot are actually Cin' and Sum'

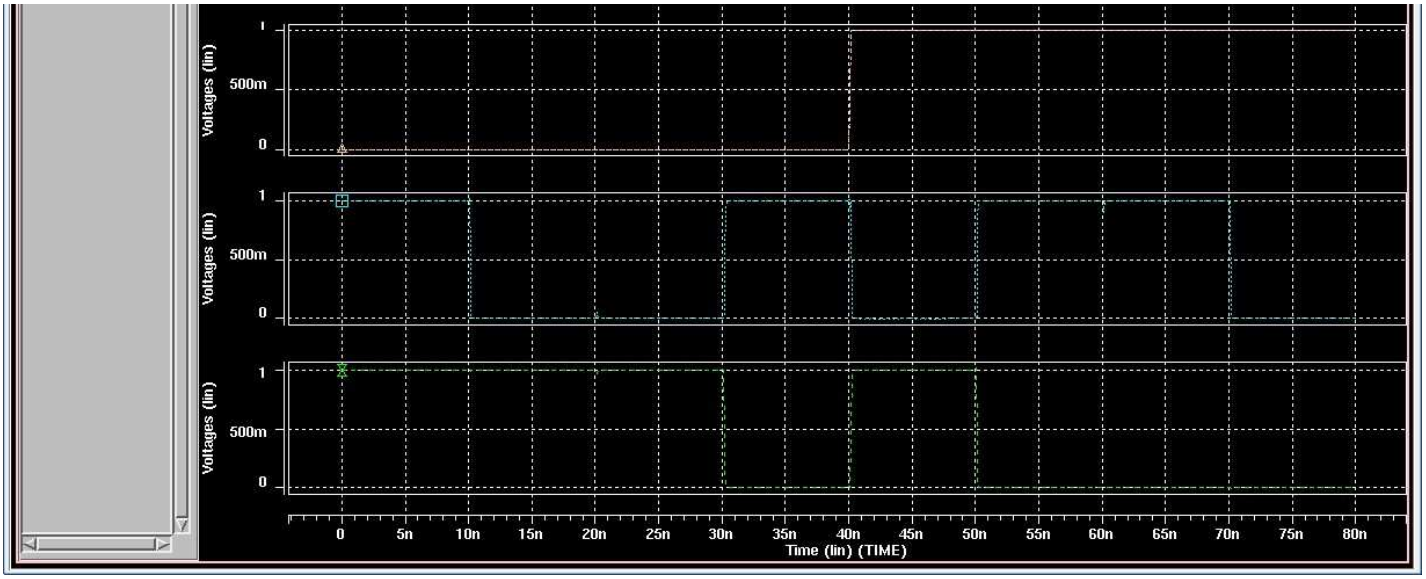

Figure 19. Awaves Output Test Waveform

Files Related to the D Flip Flop:

Description	Link
Max Layout	mirror-adder-cmos.max
HSpice	mirror-adder-cmos.sp
Inputs	mirror-adder-cmos.hsp
Measures	mirror-adder-cmos.mto

Dynamic CMOS 1 Bit Mirror Adder:

The prototype is a 1 bit full mirror adder designed in dynamic CMOS.

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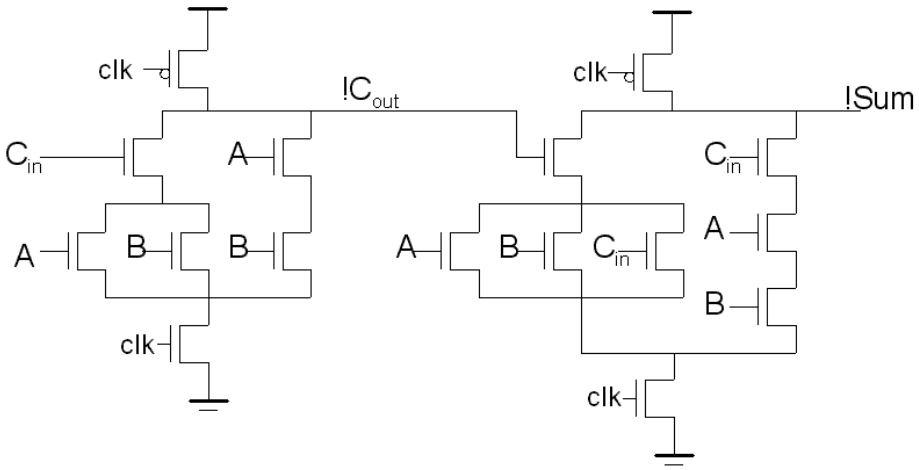

Figure 20. The Dynamic Mirror Adder

Inputs and Outputs

Type	Name	Description
Input	A	Data Input
Input	B	Data Input
Input	Cin	Carry In
Input	Clock	Clock Signal
Output	Cout	Carry Out
Output	Sum	Sum

Specifications

Measure	Value
Width	13.9
Length	23.19
Avg Power	5.94µW
Peak Power	1.53mW
Supply Voltage	1V

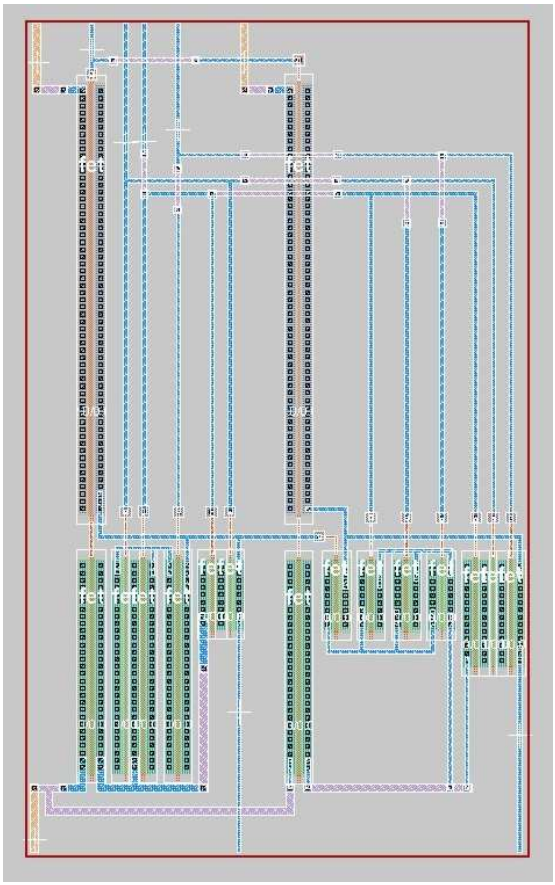

Figure 21. The Dynamic Mirror Adder VLSI Design

The following graph shows the dynamic adder operating correctly, for all of the possible inputs at a supply voltage of 1V. Speed was not considered because the design is going to focus on achieving to lowest power which the greatest speed for an operating block of 8 units.

Note: Cin and Sum in the plot are actually Cin' and Sum

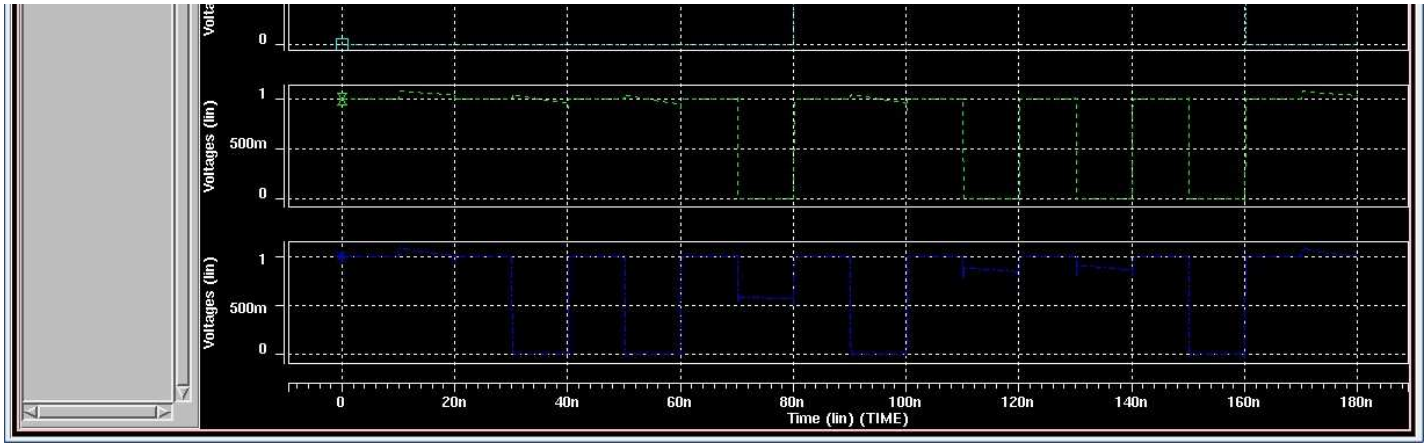

Figure 22. Awaves Output Test Waveform

Files Related to the D Flip Flop:

Description	Link
Max Layout	mirror-adder-dynamic.max
HSpice	mirror-adder-dynamic.sp
Inputs	mirror-adder-dynamic.hsp
Measures	mirror-adder-dynamic.mto

Comparison

So far the CMOS design appears to consume the least amount of power. To design this part of a music player, most power use is going to come from the dynamic power. As a result I expect to see the CMOS's dynamic power to be less, but the dynamic circuit should use less static power.