Project Specifications:

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Subthreshold Data Path Circuit Design:
Two Implementations of Low Power Simple Adder

Project Specification:

For this project I will be doing two different implementations of a simple 8 bit program controller. The circuits will have the same topology, but one adder will be built using static CMOS construction, the other using dynamic CMOS construction. The circuit will be an 8 bit adder with one input connected to a static input of 00000001, the other input will be connected to a 2-to-1 flip-flopped Mux. The Mux will control whether the input to the adder will be the previous sum or a jump to value. This is designed to simulate the program control that would be required to continuously read from a memory address such as in a portable music player, but have the ability to skip(jump) to the next song in memory.

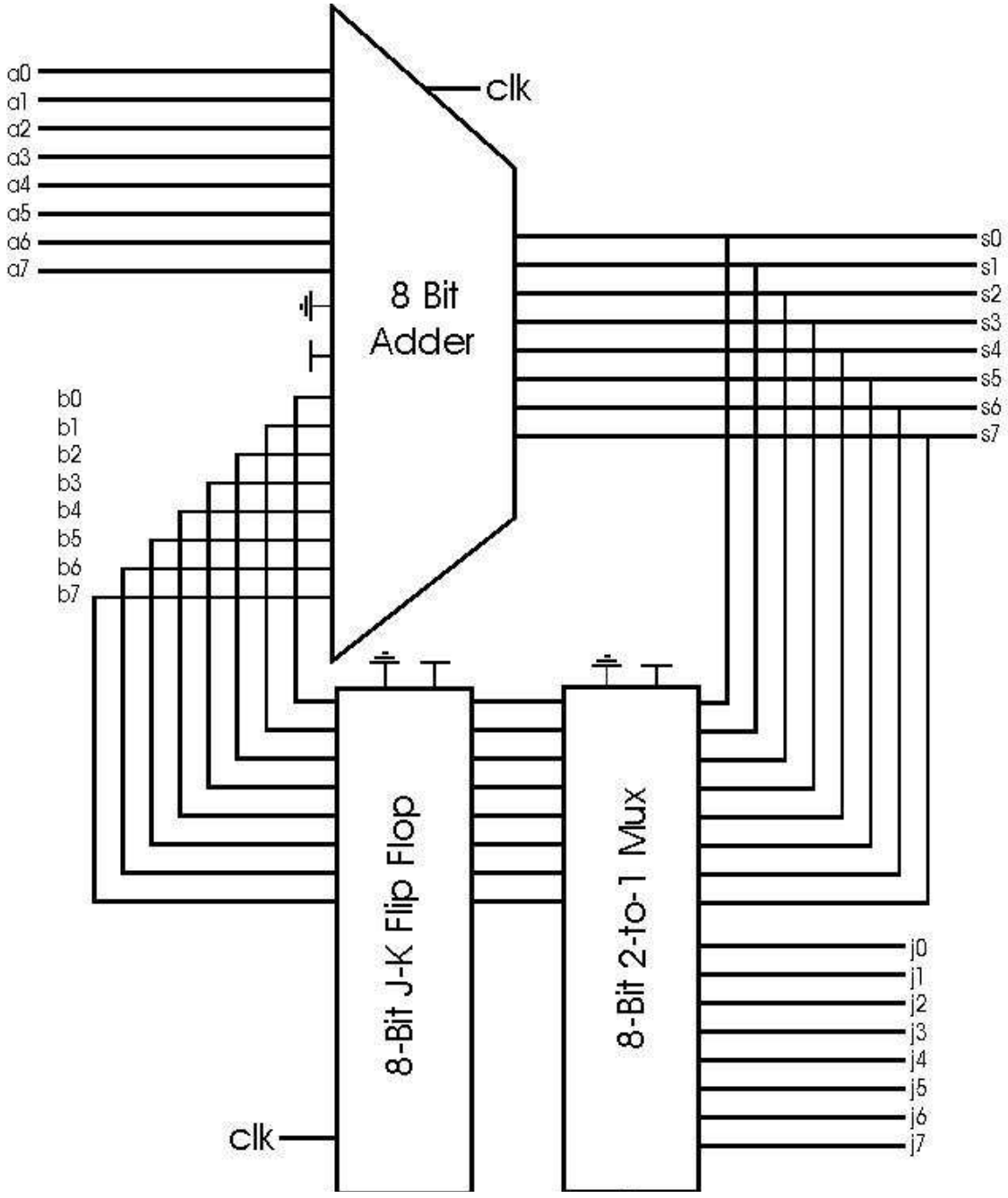


Figure 3. Circuit Topology: 8 Bit Adder With 2-to-1 Mux and D Flip Flop Allowing For Jump

The static versus dynamic circuits should be an interesting comparison. The static CMOS design will only dissipate dynamic(switching) power as there is no path from supply voltage to ground. However, the number of transistors in the static CMOS will be almost twice as many as the dynamic CMOS implementation. Static CMOS with a fan in of N requires 2N transistors. This may require more power to switch more transistors.

The dynamic CMOS will only require N+2 transistors for an input fan-in of N, which is substantially lower. The dynamic CMOS also consumes only dynamic power, however the overall power dissipation can be much higher. Finally the dynamic CMOS should be faster due to the reduced load capacitance attributed to the lower number of transistors per gate. Also the dynamic gates do not have short circuit current, and all the current provided by the pull-down transistors go towards discharging the load capacitance. It will also require the clock, and possibly a skewed clock, be sent to every block in the circuit.

It may be possible that some sections of the design work best in static CMOS and some in dynamic CMOS. The circuit is going to be laid out in a modular form in MAX, so If testing of the components proves that some parts should be static, some dynamic, a third "uber" circuit will be constructed in the prototype phase and analyzed.

Block Specification:

8bit 2-to-1 Multiplexor:

This will allow us to select whether the input will be a jump or the previous sum to keep counting. It will be a basic 8 bit 2-to-1 Multiplexor Designed in Static and Dynamic CMOS respectively.

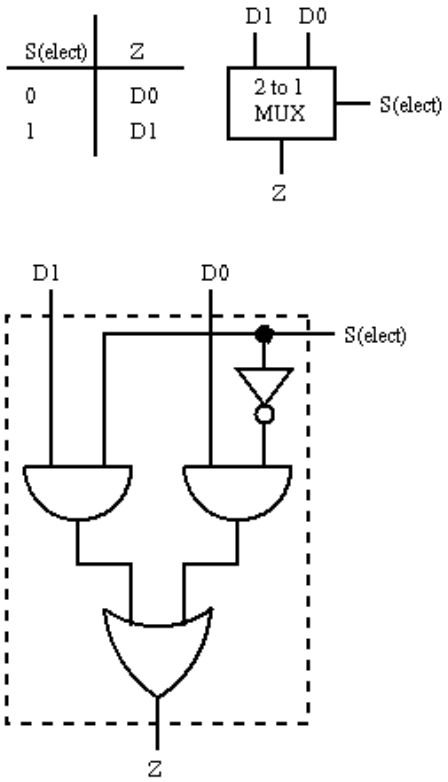


Figure 4. 2-to-1 Mux (Choi)

J-K Master-Slave Flip Flop:

This block will keep the adder functioning at the speed of the clock, and keep the output from reaching the input before the next clock edge.

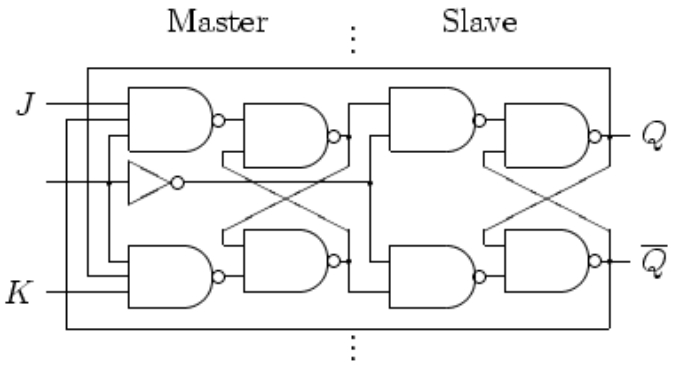


Figure 5. J-K Master Slave Flip Flop(Gillard)

8-Bit Full Adder:

I will using the ripple carry adder to try and reduce the number of transistors used, and based on the fact that the adder will be used much like a counter, not much carrying will have to propogate before the correct answer is acheived. The text suggests that if a more complex adder is used then the amount of power required to keep a desired performance could be lowered. However, in this experiment we will test only the advantages of dynamic vs. static implementations.

Because the inverting property of an adder:

S'(A,B,Cin)= S(A', B' Cin') and C'(A,B,Cin) = C(A', B', C') the inverters in the carry path become unnessary.

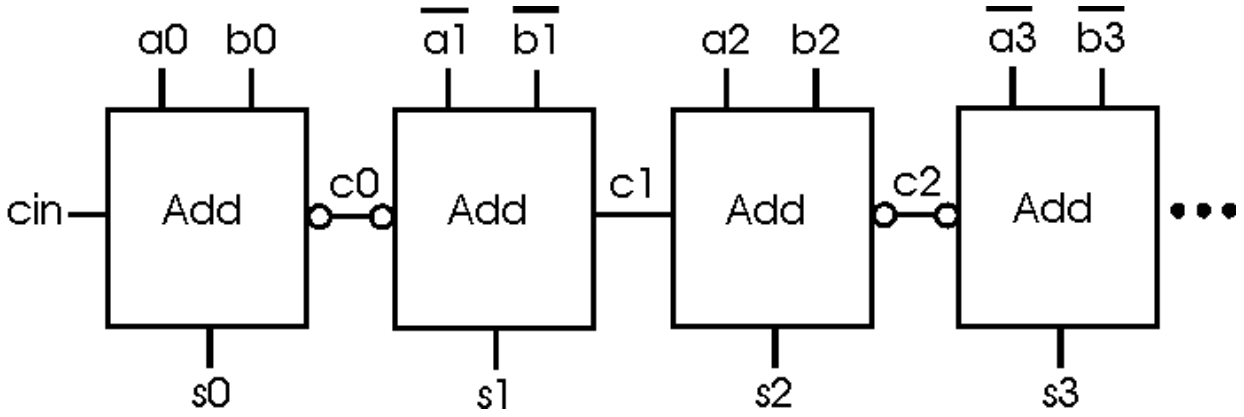
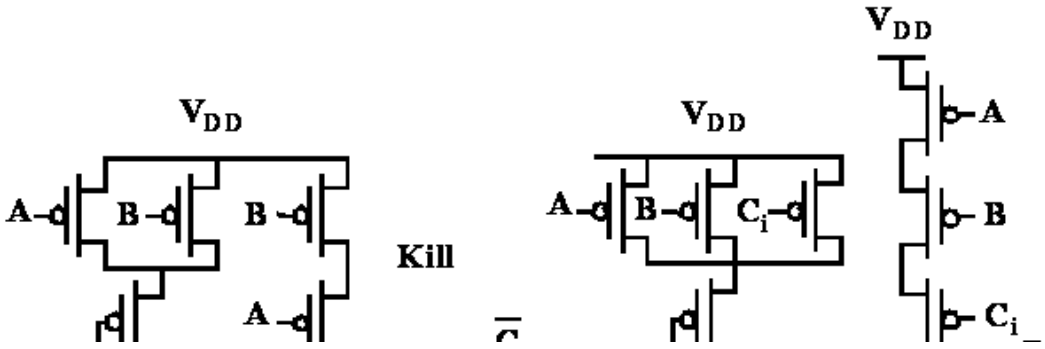


Figure 6. Full Adder Chain

For the static CMOS implementation a mirror adder will be used. The mirror adder is an improved design of the tradition full bit adder. It uses only 24 transistors and the those concerning the carry are placed closed to the output of the gate. Only the transistors in the carry stage of the circuit have to be optimized for speed. The most critical issue in the layout of the cell is the minimization of the capacitance at carry out.



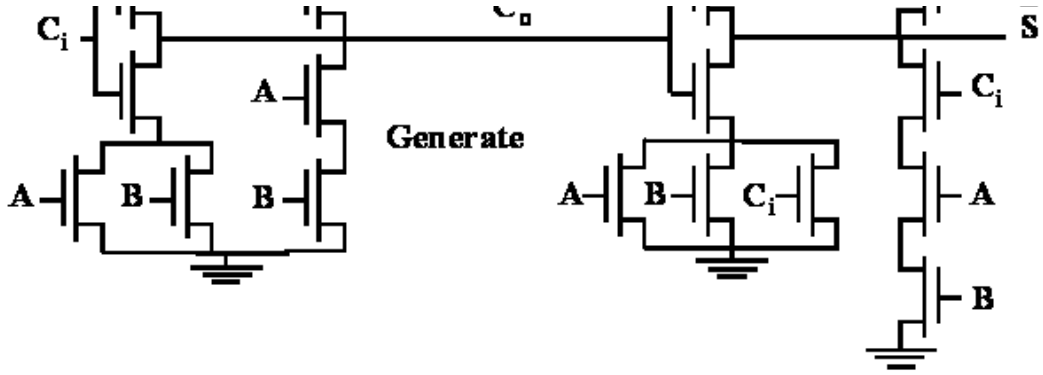


Figure 7. The Mirror Adder

For the dynamic design the mirror adder is stripped of it's pull up network and replaced with a clocked precharge transistor and an extra evaluation transistor on the pull down network.

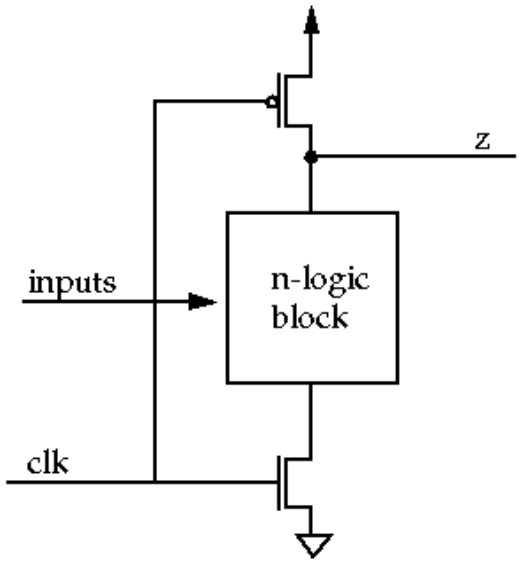


Figure 8. Basic Dynamic CMOS Design

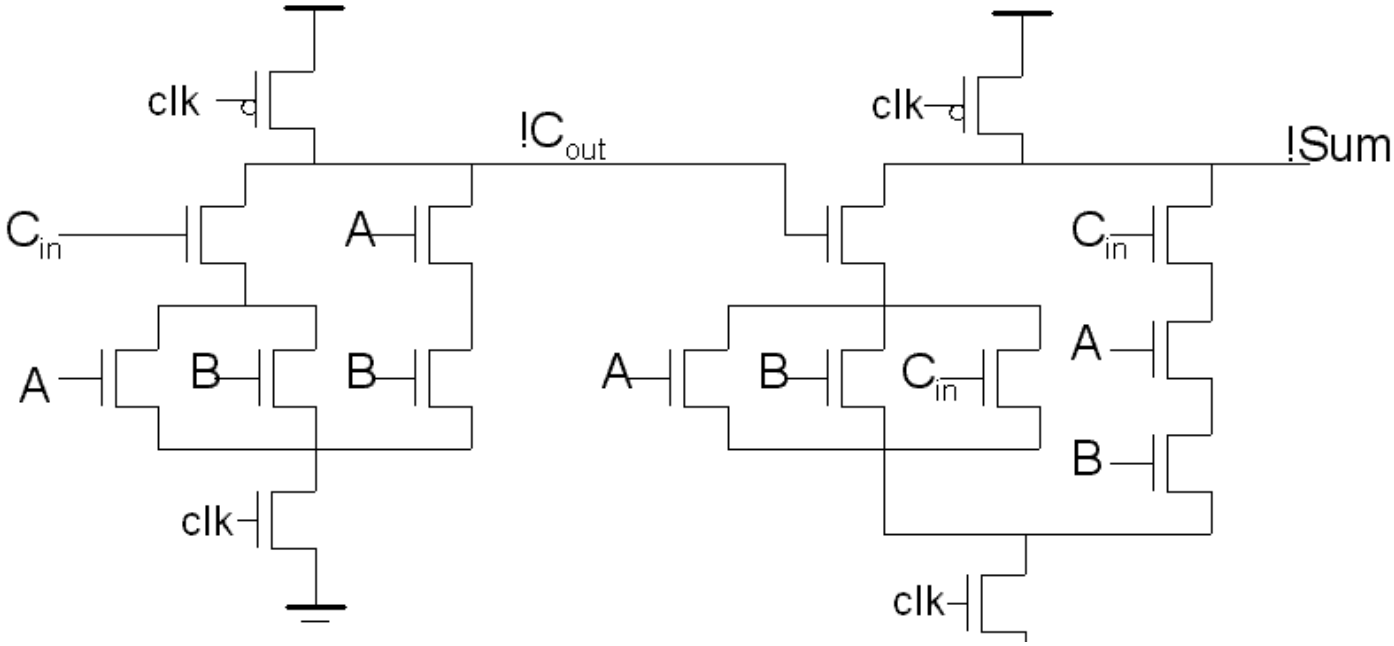


Figure 9. Dynamic CMOS Adder

Sources:

Paul Gillard
http://web.cs.mun.ca/~paul/cs3724/material/web/notes/node14.html

Kyusun Choi
http://www.cse.psu.edu/~cg471/